Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **C**
4. **D**
5. **E**
6. **F**
7. **GND**
8. **Y**
9. **NC**
10. **NC**
11. **G**
12. **H**
13. **NC**
14. **VCC**

**.039”**

**12 11**

**8**

**7**

**14**

**1**

**.049”**

**2 3 4 5 6**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential:**

**Mask Ref: S30B**

**APPROVED BY: KW DIE SIZE .039” X .049” DATE: 10/6/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54S30**

**DG 10.1.2**

#### Rev B, 7/19/02